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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/964,247	09/26/2001	Nobuo Sasaki	SCEI 3.0-086	1848

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EXAMINER	
HOANG, PHUONG N	
ART UNIT	**PAPER NUMBER**
2126	

DATE MAILED: 12/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/964,247	SASAKI, NOBUO	
	Examin r	Art Unit	
	Phuong N. Hoang	2126	

-- The MAILING DATE of this c mmunication appears on the cover sheet with the correspondence address --

Period f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 September 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 September 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/29/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 18 are pending in the application.

2. It is noted that although the present application does contain line numbers in the specification and claims, the line numbers in the claims do not correspond to the preferred format. The preferred format is to number each line of every claim, with each claim beginning line 1. For ease of reference by both the Examiner and Applicant all future correspondence should include the recommend line numbering.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1 - 18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a. The following terms lack proper antecedent basis:

i. the processor – claim 3;

ii. the respective outputs, the template – claim 9;

iii. the calculation result – claim 10;

iv. said plurality of processors, some of the processing results, the result of processing – claim 14;

v. the processing result – claims 16, 17, and 18;

b. The following claim languages are not clearly understood:

i. As to claims 1 – 15, the lack and, in many case, misuse of punctuation make it very difficult to determine exactly which processors are connected to which processors; and the controller or the processor, does the specific functionality.

ii. As to claim 1, line 6, it is uncertainly whether "each processor" refers to one of said plurality of processors.

iii. As to claims 16 - 18, lines 1 – 2, it is not clearly understood what two-way communication between a plurality of data processing means" (i.e., is it communication between a plurality of data processing and a controller). "between.....and" should be in the same sentence; lines 4 – 5, at least one said data processing means (i.e., is it at least one of said data processing means).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1 - 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Umeda, EP 0360527 A2.

7. Umeda was cited by applicant in IDS filed on 1/29/02.

8. **As to claim 1**, Umeda teaches the invention substantially as claimed including a multi-processor system comprising:

a plurality of processors (a plurality of processors 14, fig. 1 and col. 4 lines 55 - col. 4 line 15) for performing data processing process data; and

a controller for broadcasting data (controller 10 send control signals and broadcasts global data to all processors, fig. 1 and col. 4 lines 20 - 43 and col. 5 lines 29 - 36) including data used in data processing to said plurality of processors, wherein each of said plurality of processors manages (managing event signal designating an address signal for data to be processed by a processor element, col. 3 lines 5 - 20) data necessary for data processing to be performed by each processor.

Umeda does not explicitly teach the step of sorting out data necessary for processing.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to recognize that in order for Umeda's system to properly perform

its function, managing data to be processing would involve sorting the data to be processed.

9. **As to claim 2**, Umeda teaches the steps of wherein said controller obtains a result of processing from each processor (output data to the controller 10, col. 2 lines 25 - 45, col. 4 lines 20 - 35, col. 5 lines 1 - 8 and col. 8 lines 20 - 45) that has performed data processing, and broadcasts the obtained result of processing to all processors (the resultant data is returned to all of the processor elements, col. 1 lines 29 - col. 2 lines 5).

10. **As to claim 3**, Umeda teaches the step of wherein each of said plurality of processors is assigned identification data (address of the data to be processed by the processors, col. 10 lines 25 - 55), for identifying each processor, said controller generates broadcast data where identification data of the processor as a result obtaining source is added (add, col. 5 lines 10 – 20) to the result of processing and broadcasts said data and said plurality of processors sorts out said result of processing necessary for data processing that each processor should perform at next timing based (next clock, col. 5 lines 8 - 48) on said identification data.

11. **As to claim 4,** Umeda teaches the step of sort mechanism (col. 2 lines 30 - 40) for obtaining identification data from a plurality of processors and to send obtained identification data to said controller in a given sequence (sequence, col. 6 lines 20 - 25)

wherein said controller is configured to obtain said result of processing based on identification data received from said sort mechanism.

12. **As to claim 5**, Umeda teaches the step comprising of means for generating priority data (priority order, col. 6 lines 5 - 25) that fixes a reading sequence of said result of processing to be performed by said controller, wherein the processor that has finished data processing is configured to send said sort mechanism identification data of the processor and said priority data about the processing, said sort mechanism is configured to determine a sequence (sequencer 21, col. 6 lines 20 - 30) of sending said identification data based on said priority data.

13. **As to claim 6**, Umeda teaches the step comprising of wherein said sort mechanism includes the same number of registers (each of the processors elements comprises a data register .... in response to the order from the controller 10, col. 4, lines 43 - 50) as said processors, means for recording said identification data from the respective processors, a comparator (comparator, col. 15, lines 20 – 30 and col. 16, lines 5 – 24) for performing a comparison between said priority data to determine sequence of identification data recorded in the respective registers.

14. **As to claim 7**, Umeda teaches the step of wherein said controller includes memory for storing obtained result in said memory (control memory 11, col. 4, lines 23 – 25), and data generating means for reading (reading out information in the control

memory 11, col. 6, lines 20 – 25) said result of processing stored in said memory to generate said broadcast data that includes said result of processing and said received identification data.

15. **As to claim 8**, Umeda teaches the steps of wherein each of said plurality of processors includes a data processing mechanism for determining whether or not data necessary for data processing that is performed by each processor is included in said broadcast data (process data based on a based address determined by the event signal to be managed by the scheduling circuit and an address signal applied from the controller, col. 3, lines 15 - 20) to sort out only the data when said necessary data is included therein and perform data processing means for sending said controller the result of data processing performed by said data processing mechanism and identification of each processor according to a request from said controller, and means for sending said sort mechanism notifying (signal ... complete processing, col. 5, lines 30 - 37) when ending data processing.

16. **As to claim 9**, Umeda teaches multiprocessor system comprising:

a plurality of processors (a plurality of processors 14, fig. 1, and col. 4, lines 55 - col. 4 line 15) for each holding template data to be compared (comparator, col. 15, lines 20 – 35 and col. 16, lines 5 – 20) with data to be input;

a controller for broadcasting (controller 10 send control signals and broadcasts global data to all processors, fig. 1, and col. 4, lines 20 – 43, and col. 5, lines 29 - 36),

each of said plurality of processors calculates a differential value (max or min, col. 9 - col. 10, line 20) between said input data broadcasted by said controller and the template data hold by each processor, and sends said comparison mechanism a pair of data including said calculated differential value (the data calculated in the final stage is output to the global data register 12 in the controller 10, col. 5, lines 1 – 7), and said comparison mechanism selects any one of differential values (max or min value, col. 9 - col. 10, lines 20) based on said differential values received from the respective processors (controller 10 then send the control signal "max" or "min", col. 5, lines 55 – 57) and sends said controller identification data (always send identification data to be recognize from which processor, col. 10 lines 25 – 45) paired with the selected differential value (signal, col. 10 lines 25 – 45), and said controller specifies one processor from said plurality of processors based on the identification data received from said comparison mechanism (the essential processor element can be selected in response to "max" or "min", col. 6 lines 1 – 9).

Umeda teaches identification data for each processor (col. 10 lines 25 - 55).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to recognize that the identification data of each processor is purposed the hold different template data.

17. **As to claim 10**, this is the system claim of claim 1. See rejection for claim 1 above. Further, Umeda teaches a sum circuit (add calculation circuit, col. 9 lines 5 –

35) for calculating the sum of results of data processing performed by said plurality of processors.

18. **As to claim 11**, Umeda teaches the step of wherein at least some of said plurality of processors are connected to each other (PEs are connected to each other, fig. 1 and col. 6 lines 10 – 20) in a ring format via common memory, and are configured such that transmission/ reception of data between the processors connected in a ring format is performed via said common memory (memory, col. 11 lines 5 – 30).

19. **As to claims 12 and 13**, see rejection for claim 11 above.

20. **As to claim 14**, this is the apparatus claim of claim 2. See rejection for claim 2 above. Further, Umeda teaches the step of the result is in a given order (sequence, col. 6 lines 20 - 30), selecting only some of the processing results (the essential processor can be selected, col. 5 lines 50 – col. 6 lines 5).

21. **As to claim 15**, this is the system claim of claim 1. See rejection for claim 1 above.

22. **As to claim 16**, Umeda teaches a data processing system that performs two-way communication between a plurality of data processing means that performs data processing, said data processing system comprising

means for specifying at least one said data processing means (the essential processor can be selected, col. 5 lines 50 – col. 6 lines 5) to generate broadcast data including identification information (address of the data to be processed by the processors, col. 10 lines 25 - 55) of said generate broadcast data broadcasts global data to all processors, fig. 1 and col. 4 lines 20 - 43 and col. 5 lines 29 - 36);

means for obtaining a result of data processing performed by the corresponding data processing means (output data to the controller 10, col. 2 lines 25 - 45, col. 4 lines 20 - 35, col. 5 lines 1 - 8 and col. 8 lines 20 - 45); and

means for including the processing result received in said broadcast data to broadcast said broadcast data to each of said plurality of data processing means (the resultant data is returned to all of the processor elements, col. 1 lines 29 - col. 2 lines 5).

23. **As to claim 17**, this is the program claim of claim 16. See rejection for claim 16 above.

24. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Umeda, EP 0360527 A2 in view of Fiduccia, US patent no. 4,739,476.

25. **As to claim 18**, this is the system claim of claim 16. See rejection for claim 16 above.

Umeda does not explicitly teach a semiconductor device.

Fiduccia teaches a semiconductor device (semiconductor circuit, col. 1 lines 53 – 65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Umeda and Fiduccia's system because Fiduccia's semiconductor device would improve the performance of Umeda's system in processing the SIMD architecture.

Conclusion

26. The prior art made of record but not relied upon request is considered to be pertinent to applicant's disclosure.

Koyanagi, US patent no. 6,516,403, demonstrating a system having a controller for controlling over all operation, the system including a plurality or processors.

Rockoff, US patent no. 5,511,212, demonstrating a single instruction-stream multiple data-stream computer system.

Wilkinson, US patent no. 5,805,915, demonstrating a SIMIMD array of processors.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phuong N. Hoang whose telephone number is

(571)272-3763. The examiner can normally be reached on Monday - Friday 9:00 am to 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571)272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ph
December 10, 2004

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